## CLAIMS

What is claimed is:

1. A system for testing an abstracted timing model representative of an integrated circuit design comprising:

a controller;

memory associated with said controller for storing electronic format instructions;

said controller is configured to:

receive a reference timing value;

Receive an extracted model timing value;

determine difference between said reference timing value and said extracted model timing value;

determine whether said difference is within a predetermined permissible range; and

output indicgfation of success if said difference falls within said predetermined permissible range.

2. The system of claim 1 wherein said memory is further configured to store data representing said predetermined permissible range.

3. The system of claim 1 wherein said controller is configured in accordance with said electronic format instructions stored on said memory.

4. The system of claim 1 wherein said controller is further configured to generate a first structural model representative of a signal path.

5. The system of claim 1 wherein said reference timing value is representative of the time required for a predetermined signal to propagate thru a data path represented by said first structural model and extracted parasitic values.

6. The system of claim 5 wherein said extracted model timing is representative of the time required for said predetermined signal to propagate thru a data path represented by a predetermined extracted timing model.

7. The system of claim 6 wherein said controller is further configured to generate said reference timing value.

8. The system of claim 7 wherein said controller is further configured to generate said extracted model timing value.

9. The system of claim 5 wherein said controller is further configured to generate said predetermined strucutral model and to extract said parasitic values.

10. The system of claim 6 wherein said controller is further configured to generate said predetermined extracted timing model.

11. A method of testing an abstracted timing model, comprising the steps of:

receiving a reference timing value;

receiving an extracted model timing value;

determining the difference between said reference timing value and said extracted model timing value;

determining whether said difference is within a predetermined permissible range; and

outputting an indication of success if said difference falls within said predetermined permissible range.

12. The method of claim 11 further comprising the step of generating said reference timing value, said reference timing value is representative of the time required for a predetermined signal to propagate thru a data path represented by a predetermined sturcutral model and extracted parasitic values.

13. The method of claim 12 further comprising the step of generating said extracted model timing value, said extracted model timing value is representative of the time required for said predetermined signal to propagate thru a data path represented by a predetermined extracted timing model.

14. The method of claim 12 further comprising the step of generating said predetermined structural model.

15. The method of claim 13 further comprising the step of generating said predetermined extracted timing model.

16. A computer program for testing an abstracted timing model, the computer program comprising:

a first code segment for receiving a reference timing value;

a second code segment for receiving an extracted model timing value;

a third code segment for determining the difference between said reference timing value and said extracted model timing value; and

a fourth code segment for outputting an indication of success if said difference falls within said predetermined permissible range

17. A computer program according to claim 16, further comprising a fifth code segment for generating said reference timing value, said reference timing value is representative of the time required for a predetermined signal to propagate thru a data path represented by a predetermined structural model and extracted parasitic values.

18. A computer program according to claim 16, further comprising a sixth code segment for generating said extracted model timing value, said extracted model timing value is representative of the time required for said predetermined signal to propagate thru a data path represented by a predetermined extracted timing model.

19. A computer program according to claim 17, further comprising a sixth code segment for generating said predetermined structural model.

20. A computer program according to claim 18, further comprising a sixth code segment for generating said predetermined extracted timing model.